AMENDMENTS TO THE CLAIMS

This listing of Claims shall replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A method of obtaining debug information, comprising:

executing a sequence of instructions by a device under test (DUT), wherein said DUT comprises a data line and a clock line;

executing the sequence of instructions by an emulator device emulating the functions of the DUT and executing the sequence of instructions in lock-step fashion with the DUT, wherein said emulator device shares a clock signal with said DUT;

the DUT conveying I/O read information to the emulator device over said data line during a data transfer phase; and

a host computer system reading real-time state and debug information from the emulator device without interrupting the DUT.

2. (Previously Presented) The method according to claim 1, wherein the DUT and the emulator device operate in a cycle comprising the data transfer phase and a control phase.

3. (Cancelled)

4. (Previously Presented) The method according to claim 1, wherein the I/O read information is conveyed to the emulator device after a start of instruction transition occurs and prior to execution of an instruction.

5. (Previously Presented) The method according to claim 4, wherein said DUT comprises a second data line, and wherein the I/O read information comprises eight bits of information, and further wherein the I/O read information is conveyed to the emulator device over said two data lines carrying four serial bits each over a time period defined by four system clock cycles.

6. (Original) The method according to claim 1, further comprising conveying interrupt vectors from the DUT to the emulator device during an interrupt service cycle.

7. (Original) The method according to claim 6, wherein the interrupt service cycle begins after assertion of an interrupt data line.

8. (Original) The method according to claim 1, wherein the DUT is selected from one of a microcontroller, a microprocessor, a microcomputer and an electronic circuit device incorporating an internal processor.

9. (Currently Amended) A method of obtaining debug information, comprising:

a) executing a sequence of instructions by a microcontroller device, wherein said microcontroller device comprises a data line and a clock line;

b) in synchronization with a), an emulator device emulating the functions of the microcontroller and executing the sequence of instructions in lock-step fashion with the microcontroller, wherein said emulator device shares a clock signal with said microcontroller device;

c) the microcontroller conveying I/O read information to the emulator

device;

d) a host computer system reading real-time state and debug information from the emulator without interrupting the microcontroller; and

e) conveying interrupt vectors from the microcontroller to the emulator device during an interrupt service cycle.

10. (Original) The method according to claim 9, wherein the microcontroller and the emulator device operate in a cycle comprising a data transfer phase and a control phase.

11. (Original) The method according to claim 10, wherein the I/O read information is conveyed to the emulator device during the data transfer phase.

12. (Original) The method according to claim 11, wherein the I/O read information is conveyed to the emulator device after a start of instruction transition occurs and prior to execution of an instruction.

13. (Previously Presented) The method according to claim 12, wherein said microcontroller comprises a second data line, and wherein the I/O read information comprises eight bits of information, and wherein the I/O read information is conveyed to the emulator device over said two data lines carrying four serial bits each over a time period defined by four system clock cycles.

14. (Cancelled)

15. (Previously Presented) The method according to claim 9, wherein the interrupt service cycle begins after assertion of an interrupt data line.

16. (Currently Amended) A method of obtaining debug information, comprising:

executing a sequence of instructions by a device under test (DUT), wherein said DUT comprises two data lines and a clock line;

executing the sequence of instructions by an emulator device emulating the functions of the DUT and executing the sequence of instructions in lock-step fashion with the DUT, wherein said emulator device shares a clock signal with said DUT;

the DUT conveying I/O read information to the emulator device;

a host computer system reading real-time state and debug information from the emulator device without interrupting the DUT;

the DUT and the emulator device operating in a cycle comprising a data transfer phase and a control phase, wherein I/O read information is conveyed to the emulator device during the data transfer phase after a start of instruction transition occurs and prior to execution of an instruction;

wherein the I/O read information comprises eight bits of information, and wherein the I/O read information is conveyed to the emulator device over said two data lines carrying four serial bits each over a time period defined by four system clock cycles; and

conveying interrupt vectors from the DUT to the emulator device during an interrupt service cycle, with the interrupt service cycle begins after assertion of an interrupt data line.

17. (Original) The method according to claim 16, wherein the DUT is selected from one of a microcontroller, a microprocessor, a microcomputer and an electronic circuit device incorporating an internal processor.